WHAT IS CLAIMED IS:

1. A method of processing a memory read request from a central processing unit (CPU) of a microprocessor, the method comprising:

retrieving a cache tag associated with the memory read request from a cache memory bank that is external to the microprocessor, wherein the cache memory bank stores cache tags and cache data in separate memory locations;

within the microprocessor, comparing the cache tag to a memory address associated with the memory read request to assess whether data requested by the CPU resides within the cache memory bank, and

subsequent to retrieving the cache tag from the cache memory bank, accessing the cache memory bank to retrieve the cache data associated with the memory read request.

2. The method of Claim 1, wherein the step of accessing the cache memory bank to retrieve said data overlaps in time with said step of comparing the cache tag to the memory address,

3. The method of Claim 1, wherein the cache tag and the data are retrieved from the cache memory bank over a shared data/address bus that connects the microprocessor to the cache memory bank.

4. The method of Claim 1, further comprising comparing the cache tag to the memory address within a system controller device that interfaces the microprocessor to a main memory.

5. The method of Claim 1, wherein the method comprises mapping the memory address into a cache tag address and a cache data address that are sequentially provided to the cache memory bank to retrieve the cache tag and the cache data therefrom.

6. A microprocessor that operates according to the method of Claim 1.

7. A microprocessor that operates according to the method of Claim 1, wherein the microprocessor includes an address transformation circuit that converts the memory address into cache memory addresses for reading the cache tag and cache data.

8. A microprocessor system, comprising:

a bank of general purpose random access memory that stores both cache tags and cache data in separate memory locations; and

a microprocessor connected to the bank of general purpose random access memory, and configured to use the bank of general purpose random access memory as an external cache memory;

wherein the microprocessor is configured to retrieve a cache tag from the bank of general purpose random access memory before retrieving corresponding cache data from the bank of general purpose random access memory.

9. The microprocessor system of Claim 8, wherein the microprocessor implements an address mapping function to map a memory address into a cache tag address and a cache data address for retrieving the cache tag and cache data from the bank of general purpose random access memory.

10. The microprocessor system of Claim 8, wherein the microprocessor retrieves cache tags and cache data from the bank of general purpose random access memory over a shared address/data bus.

11. The microprocessor system of Claim 8, wherein the microprocessor includes a comparison circuit that compares the cache tag to an associated memory address to determine whether data requested by a CPU of the microprocessor resides within the bank of general purpose random access memory.